A 1-10GHz 0.18μm-CMOS Chipset For Multi-Mode Wireless Applications

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Abstract---- Performance results for a 1-10GHz chipset developed in a low-cost two-metal 0.18μm-CMOS technology are described. The developed chips include RF and IF amplifiers, down- and up-mixers, VCO, and receiver/transmitter circuits. Each chip's circuit parameters as well as transistors gate widths are optimized for maximum frequency of operation. The receiver and transmitter chips have a conversion gain higher than 25dB over 2.4-5.8GHz, and higher than 16dB for any other frequency within 1-10GHz.

INTRODUCTION

Recent advances in wireless technology and its application to a variety of systems including 2.4GHz wide band code division multiple access/Bluetooth and 5.8GHz wireless local area network/HIPERLAN have urged development of low-cost RF chips with possibility of both frequency range coverage for dual-mode application. To meet the cost issue, selection of proper device technology is crucial. Feasibility of BiCMOS technology at multi-GHz frequencies has been already described [1]-[4], which is, however, dominated by performance of the bipolar device. With gate-length reduction, CMOS technology has shown potential to provide low cost RF chips with possibility of integration with the IF and baseband counterparts to realize a system-on-chip solution. The authors have previously reported a 0.25μm-CMOS chip operating at 2.4GHz [5]. Recently, a 0.25μm-CMOS radio transceiver chipset has been reported which operates at 5GHz band [6]. The chipset, however, has an over-all receive conversion gain of 8.7dB with 114mW/120mW power dissipation during the receive/transmit mode, and is based on a 5-level metal technology. The present paper describes an RF transceiver chipset exhibiting receive/transmit conversion gain of higher than 24dB for 2.4GHz-5.8GHz band, and higher than 16dB for any other frequency over 1-10GHz with a receive/transmit power dissipation of 87mW/75mW using a low-cost 2-level metal 0.18μm-CMOS process.

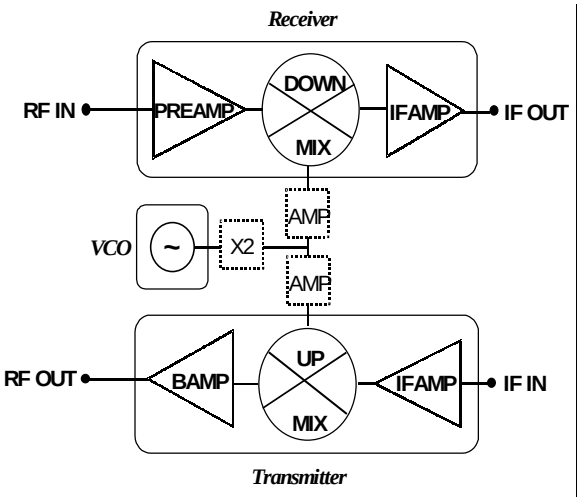

Fig. 1 CMOS transceiver block diagram.

DESIGN ISSUES AND PERFORMANCE

Fig. 1 shows the RF transceiver block diagram consisting of a receiver with a preamplifier, a down - mixer, and an IF amplifier, a transmitter with an IF amplifier, an up-mixer, and a buffer amplifier, and a VCO with a frequency doubler and amplifiers. Each individual circuit was designed for maximum frequency of operation with a nominal supply voltage of

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3V. Measured f_T and f_{max} for a 50μm x 0.18μm NMOS transistor are 32GHz and 42GHz, respectively, at a drain voltage and current of 1V and 2mA. To enhance high frequency performance, an optimum layout patterning was implemented. The design avoids use of lossy series capacitors as much as possible. Moreover, we have used on-chip inductors only when the quality factor is not an issue regarding circuit performance, as the low-cost process has only a thin two-metal wiring system.

A. Preamplifier

The preamplifier, shown in Fig. 2, employs a 2-stage common source with an output source follower buffer stage. No specific on-chip frequency selective matching network was employed to facilitate a broadband amplification. However, application of the source follower stage assures a satisfactory output matching regardless of the operation frequency. The gate width for the common source MOSFETs is 50μm to enhance high frequency operation, and is 100μm for the buffer MOSFET to enhance output power. Fig. 3 depicts measured small signal S-parameters and noise figure for the amplifier. In a 50Ω-system, the amplifier has a linear power gain of 22 dB at 2.4GHz, 12dB at 5.8GHz, 7.5dB at 8.4GHz and 2.5dB at 12GHz with a noise figure less than 5 dB over 2-7GHz, at a supply voltage and current of 2.9V and 8mA. We believe incorporation of an external input matching network can furthermore improve amplifier performance. On the other hand, the amplifier has an output 1-dB gain compression point of –7dBm and an output third order intermodulation point of 5.5dBm at 5.8GHz. The same structure has been used for the buffer amplifier in the transmitter.

B. IF Amplifier

The IF amplifier has a circuit topology similar to that of preamplifier but with an input series inductor and shunt capacitor to achieve a low-pass filtering feature. Gate width for each device is 200 μm. The amplifier has a power gain of higher than 20dB, and a noise figure of less than 6dB over 45MHz to 800MHz for a supply voltage

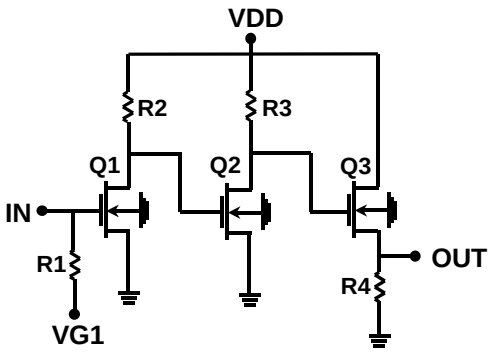


Fig. 2 Preamplifier schematic diagram.

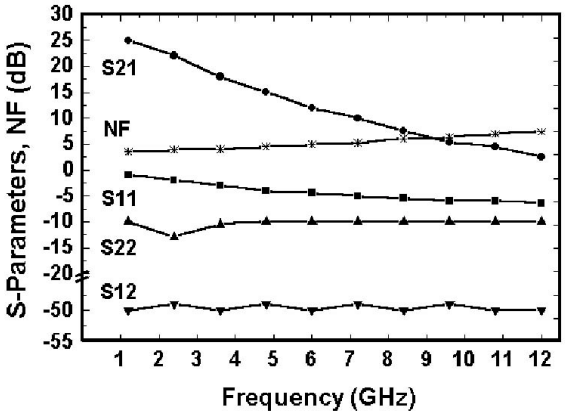


Fig. 3 S-parameters and NF for preamplifier.

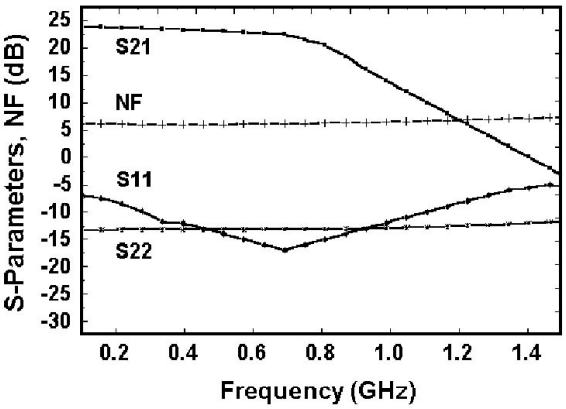


Fig. 4 S-parameters and NF for IF amplifier.

and current of 2.7V and 6mA. Fig. 4 depicts the IF amplifier's gain and noise performance.

C. Mixers

An equivalent circuit for the mixers used in the receiver and transmitter chips is shown in Fig. 5. The mixer is of a cascode type where two transistors Q1 and Q2 are connected in series, and LO and RF (or IF) signals are inputted through the gate terminal of these transistors. The resultant output IF (or RF) signal is extracted from the drain terminal of Q3 that is used for conversion gain enhancement. A cascode type mixer has the advantage of a low supply voltage operation, better input port-to-port isolation, and higher linearity. To enhance the mixing effect, Q2 is biased at a relatively low drain-source voltage. Except the inductors L1 and/or L2, no particular matching network has been employed to achieve a broadband operation. Gate width for Q1 and Q2 is 100μm, and for Q3 is 300μm. Depending on whether the mixer is used in the receiver or transmitter, load resistors R3 and R4 are optimized accordingly. As shown in Fig. 6, for a supply voltage and current of 3V and 15.5mA, the down-mixer exhibits a conversion gain of higher than 13dB for an RF frequency of up to 6GHz. The up-mixer, on the other hand, has a conversion gain higher than 8dB up to 7.5GHz, for a supply voltage and current of 2.7V and 3.5mA. At 5.8GHz, the double-sideband noise figure for the down- and up-mixers is, 11dB and 8dB, respectively. The up-mixer has an output third order intermodulation point of 5dBm at 5.8GHz.

D. VCO

The VCO, shown in Fig. 7, employs a 3-stage ring oscillator with an output source follower buffer stage. Such a structure has a wide and independent frequency and power tuning capability through VDD1 and VDD2, respectively. As shown in Fig. 8, the VCO

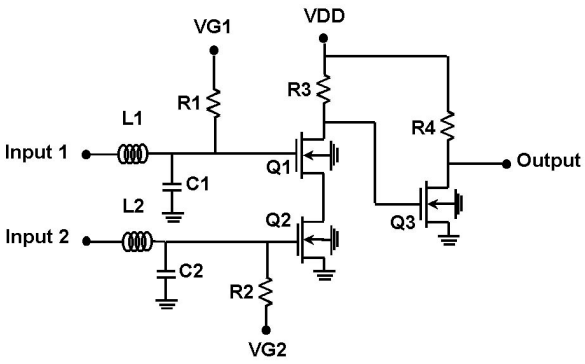


Fig. 5 Up- and down- mixer circuit topology.

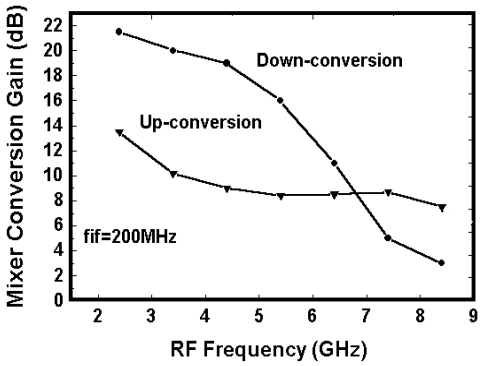


Fig. 6 Up- and down- mixer performance.

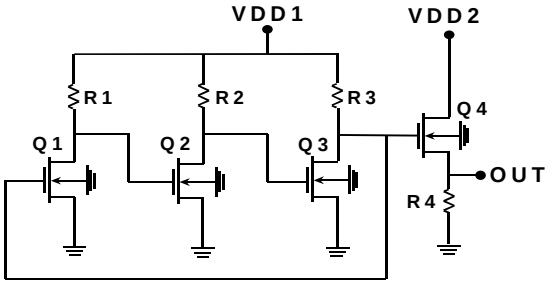


Fig. 7 VCO circuit diagram.

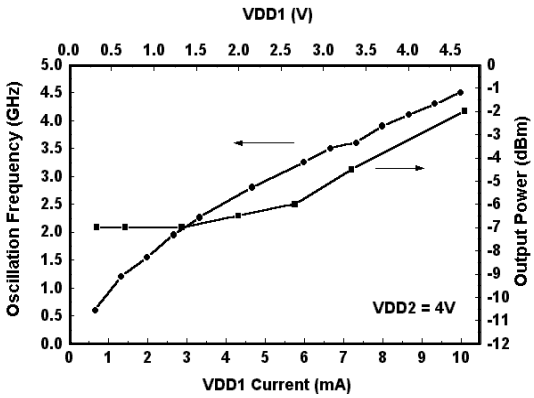


Fig. 8 VCO performance.

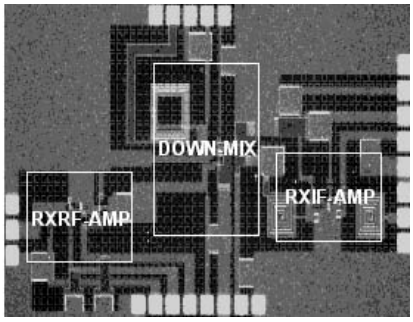
measures a continuous frequency tuning of 0.6GHz to 4.5GHz when VDD1 is changed. Output power, on the other hand, can be adjusted from –27dBm to –2dB by changing VDD2. The present VCO utilizes 300μm-width NMOS transistors. Application of devices with narrower gate width (50μm) can drastically increase the oscillation frequency.

E. Receiver and Transmitter

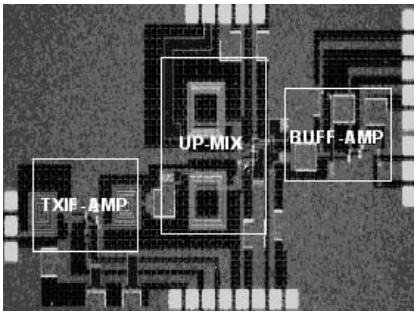
Fig. 9 shows the receiver (RX) and transmitter (TX) chips comprising the building block circuits described earlier. Chip size for both the receiver and the transmitter is 2.6mm x 1.4mm. Measured overall conversion gain for each chip is shown in Fig. 10. Both chips achieve a conversion gain that is higher than16dB for any frequency over 1-10GHz, with a maximum value of higher than 25dB at 5GHz band. Power dissipation for the receiver and transmitter is 87mW and 75mW, respectively. The receiver has a double sideband noise figure of 6.3dB, and the transmitter has an output 1-dB gain compression point of –7dBm at 5.8GHz.

CONCLUSIONS

State-of-the-art performance for a 1-10GHz chipset developed in a low-cost two-metal 0.18μm-CMOS technology were presented.



(a)



(b)

Fig. 9 RX (a) and TX (b) chip microphotograph.

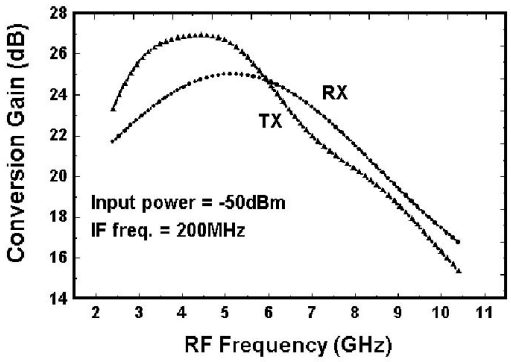


Fig. 10 RX and TX conversion gain.

ACKNOWLEDGMENTS

The authors acknowledge circuit simulation and layout design contribution by T. Drenski and L. Desclos.

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